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IN THE CLAIMS:

Please amend the claims as set forth below:

1. (Currently Amended) A processor comprising:

a plurality of segment registers including a code segment register and a stack segment register;

a circuit configured to generate an indication of a default operand size, wherein the circuit is configured to generate the default operand size responsive to a segment descriptor indicated by a segment selector stored in the code segment register, and wherein, in a first operating mode of a plurality of operating modes indicated at least in part by a content of the segment descriptor, each other one of the plurality of segment registers except for the code segment register is ignored for providing segment data; and

an execution core coupled to receive a first instruction, wherein the execution core is configured, in the first operating mode, to override the default operand size with a second operand size responsive to the first instruction having an implicit stack pointer reference.

2. (Currently Amended) The processor as recited in claim 1 further comprising ~~a segment register and~~ a ~~configuration~~ control register coupled to the circuit, wherein the ~~segment register is configured to store a segment selector locating a~~ segment descriptor located by the segment selector in the code segment register ~~which~~ includes a first operating mode indication and a second operating mode indication, and wherein the ~~configuration~~ control register is configured to store an indication, and wherein the circuit is configured to generate the indication of the default operand size responsive to the first operating mode indication, the second operating mode indication, and the indication in the ~~configuration~~ control register.

3. (Currently Amended) The processor as recited in claim 2 wherein the default operand size is 32 bits in the first operating mode.

4. (Currently Amended) The processor as recited in claim 3 wherein the circuit is further configured to generate an indication of a default address size responsive to the first operating mode indication, the second operating mode indication, and the indication in the ~~configuration~~ control register, and wherein the default address size is greater than 32 bits in the first operating mode.

5. (Original) The processor as recited in claim 3 wherein the second operand size is 64 bits.

6. (Original) The processor as recited in claim 1 wherein the execution core is configured to override the default operand size with the second operand size in an absence of an operand size override encoding for the first instruction.

7. (Original) The processor as recited in claim 1 wherein the execution core is coupled to receive a near branch instruction, and wherein the execution core is configured to override the default operand size for the near branch instruction with the second operand size.

8. (Currently Amended) A method comprising:

generating a default operand size for instructions responsive to a segment descriptor indicated by a segment selector stored in a code segment register, wherein the code segment register is one of a plurality of segment registers that also includes a stack segment register, and wherein the segment descriptor further indicates an operating mode, and wherein each other one of the plurality of segment registers except for the code segment register is ignored in the operating mode for providing segment data; and

overriding the default operand size with a second operand size for a first instruction, in the operating mode, responsive to the first instruction having an implicit stack pointer reference.

9. (Currently Amended) The method as recited in claim 8 further comprising generating ~~an~~ the operating mode responsive to a first operating mode indication ~~in a~~ in the segment descriptor and a second operating mode indication in the segment descriptor and further responsive to an indication in a ~~configuration~~ control register~~, wherein the generating the default operand size is responsive to the generating the operating mode~~.

10. (Currently Amended) The method as recited in claim 9 wherein the default operand size is 32 bits in the operating mode.

11. (Currently Amended) The method as recited in claim 10 further comprising generating a default address size responsive to the ~~generating the~~ operating mode, wherein the default address size is greater than 32 bits in the operating mode.

12. (Original) The method as recited in claim 10 wherein the second operand size is 64 bits.

13. (Original) The method as recited in claim 8 wherein the overriding the default operand size with the second operand size is performed in an absence of an operand size override encoding for the first instruction.

14. (Original) The method as recited in claim 8 further comprising overriding the default operand size for a near branch instruction with the second operand size.

15. (Currently Amended) A processor comprising:

a plurality of segment registers including a code segment register and a stack segment register;

a circuit configured to generate an indication of a default operand size, wherein the circuit is configured to generate the default operand size responsive to a segment descriptor indicated by a segment selector stored in the code segment register, and wherein, in a first operating mode of a plurality of operating modes indicated at least in part by a content of the segment descriptor, each other one of the plurality of segment registers except for the code segment register is ignored for providing segment data; and

an execution core coupled to receive a near branch instruction, wherein the execution core is configured to override the default operand size with a second operand size responsive to the near branch instruction in the first operating mode.

16. (Currently Amended) The processor as recited in claim 15 further comprising ~~a segment register and~~ a ~~configuration~~ control register coupled to the circuit, wherein the ~~segment register is configured to store a segment selector locating a~~ segment descriptor ~~which~~ located by the segment selector in the code segment register includes a first operating mode indication and a second operating mode indication, and wherein the ~~configuration~~ control register is configured to store an indication, and wherein the circuit is configured to generate the indication of the default operand size responsive to the first operating mode indication, the second operating mode indication, and the indication in the ~~configuration~~ control register.

17. (Currently Amended) The processor as recited in claim 16 wherein the default operand size is 32 bits in the first operating mode.

18. (Currently Amended) The processor as recited in claim 17 wherein the circuit is further configured to generate an indication of a default address size responsive to the first operating mode indication, the second operating mode indication, and the indication in the ~~configuration~~ control register, and wherein the default address size is greater than

32 bits in the first operating mode.

19. (Original) The processor as recited in claim 17 wherein the second operand size is 64 bits.

20. (Original) The processor as recited in claim 15 wherein the execution core is configured to override the default operand size with the second operand size in an absence of an operand size override encoding for the near branch instruction.

21. (Currently Amended) A method comprising:

generating a default operand size for instructions responsive to a segment descriptor indicated by a segment selector stored in a code segment register, wherein the code segment register is one of a plurality of segment registers that also includes a stack segment register, and wherein the segment descriptor further indicates an operating mode, and wherein each other one of the plurality of segment registers except for the code segment register is ignored in the operating mode for providing segment data; and

overriding the default operand size, in the operating mode, with a second operand size for a near branch instruction.

22. (Currently Amended) The method as recited in claim 21 further comprising generating ~~an~~ the operating mode responsive to a first operating mode indication ~~in a~~ in the segment descriptor and a second operating mode indication in the segment descriptor and further responsive to an indication in a ~~configuration~~ control register~~, wherein the generating the default operand size is responsive to the generating the operating mode~~.

23. (Currently Amended) The method as recited in claim 22 wherein the default operand size is 32 bits in the operating mode.

24. (Currently Amended) The method as recited in claim 23 further comprising generating a default address size responsive to ~~the generating~~ the operating mode, wherein the default address size is greater than 32 bits in the operating mode.

25. (Original) The method as recited in claim 23 wherein the second operand size is 64 bits.

26. (Original) The method as recited in claim 21 wherein the overriding the default operand size with the second operand size is performed in an absence of an operand size override encoding for the near branch instruction.

27. (New) The processor as recited in claim 1 wherein the default operand size is 32 bits in the first operating mode.

28. (New) The processor as recited in claim 27 wherein the circuit is further configured to generate an indication of a default address size, and wherein the default address size is greater than 32 bits in the first operating mode.

29. (New) The processor as recited in claim 27 wherein the second operand size is 64 bits.

30. (New) The method as recited in claim 8 wherein the default operand size is 32 bits in the operating mode.

31. (New) The method as recited in claim 30 further comprising generating a default address size responsive to the operating mode, wherein the default address size is greater than 32 bits in the operating mode.

32. (New) The method as recited in claim 30 wherein the second operand size is 64 bits.

33. (New) The processor as recited in claim 15 wherein the default operand size is 32

bits in the first operating mode.

34. (New) The processor as recited in claim 33 wherein the circuit is further configured to generate an indication of a default address size, and wherein the default address size is greater than 32 bits in the first operating mode..

35. (New) The processor as recited in claim 33 wherein the second operand size is 64 bits.

36. (New) The method as recited in claim 21 wherein the default operand size is 32 bits in the operating mode.

37. (New) The method as recited in claim 36 further comprising generating a default address size responsive to the operating mode, wherein the default address size is greater than 32 bits in the operating mode.

38. (New) The method as recited in claim 36 wherein the second operand size is 64 bits.

39. (New) An apparatus comprising:

a plurality of storage locations corresponding to a plurality of segment registers, wherein the plurality of segment registers include a code segment register and a stack segment register; and

a processor configured to generate an indication of a default operand size, wherein the processor is configured to generate the default operand size responsive to a segment descriptor indicated by a segment selector stored in a storage location of the plurality of storage locations that corresponds to the code segment register, and wherein, in a first operating mode of a plurality of operating modes indicated at least in part by a content of the segment descriptor, each other one of the plurality of segment registers

except for the code segment register is ignored for providing segment data, and wherein, in response to a first instruction having an implicit stack reference and the first operating mode, the processor is configured to override the default operand size with a second operand size.

40. (New) The apparatus as recited in claim 39 wherein the default operand size is 32 bits in the first operating mode.

41. (New) The apparatus as recited in claim 40 wherein the processor is further configured to generate an indication of a default address size, and wherein the default address size is greater than 32 bits in the first operating mode.

42. (New) The apparatus as recited in claim 40 wherein the second operand size is 64 bits.

43. (New) The apparatus as recited in claim 39 wherein the processor is configured to override the default operand size with the second operand size in an absence of an operand size override encoding for the first instruction.

44. (New) The apparatus as recited in claim 39 wherein the processor is configured to override the default operand size for a near branch instruction with the second operand size.

45. (New) An apparatus comprising:

a plurality of storage locations corresponding to a plurality of segment registers, wherein the plurality of segment registers include a code segment register and a stack segment register; and

a processor configured to generate an indication of a default operand size, wherein the processor is configured to generate the default operand size

responsive to a segment descriptor indicated by a segment selector stored in one of the plurality of storage locations corresponding to the code segment register, and wherein, in a first operating mode of a plurality of operating modes indicated at least in part by a content of the segment descriptor, each other one of the plurality of segment registers except for the code segment register is ignored for providing segment data, and wherein the processor is configured to override the default operand size with a second operand size responsive to a near branch instruction in the first operating mode.

46. (New) The apparatus as recited in claim 45 wherein the default operand size is 32 bits in the first operating mode.

47. (New) The apparatus as recited in claim 46 wherein the processor is further configured to generate an indication of a default address size, wherein the default address size is greater than 32 bits in the first operating mode.

48. (New) The apparatus as recited in claim 46 wherein the second operand size is 64 bits.

49. (New) The apparatus as recited in claim 45 wherein the processor is configured to override the default operand size with the second operand size in an absence of an operand size override encoding for the near branch instruction.